AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) An inter-bus communication interface device for controlling data communication between a first bus and a second bus, comprising:

a buffer in which is stored only communication data sent from a first device connected to the first bus;

a register in which is stored only communication control information concerning the communication data sent from the first device for handling the communication data, and when writing of the communication data is completed, data end information is written as the communication control information; ~~and~~

a status register storing information indicating a status of the buffer and the register, the status indicating that the buffer is full of data and that new information has been written in the register; and

a control circuit for passing the communication data stored in said buffer to a second device connected to the second bus, and passing the ~~communication control~~ data end information stored in said register to the second device, wherein the communication control information and the communication data are sent via the register and the buffer, respectively, and the second device reads out data stored in the buffer if the status register indicates that the buffer is full of data, and that new information has been written in the register, and performs an appropriate receive process according to

the control information and completes the receive process when detecting the data end information.

2. (Original) The inter-bus communication interface device as claimed in claim 1, wherein said buffer is of a type that outputs data in the order that the data are stored.

3. (Previously Presented) The inter-bus communication interface device as claimed in claim 1, wherein said buffer includes a plurality of buffer areas, said buffer areas being alternately used in storing the communication data.

4. (Original) The inter-bus communication interface device as claimed in claim 1, wherein said control circuit outputs an interrupt signal to the second device, immediately after the communication control information is stored in said register.

5. (Currently Amended) The inter-bus communication interface device as claimed in claim 1, ~~further including a status register for storing information indicative of whether or not untransmitted data exists in said register, and~~

wherein said control circuit updates the information in said status register, when new data is stored in said register, or when data in said buffer is read out by the second device.

6. (Currently Amended) An inter-bus communication interface device for controlling data communication between a first bus and a second bus, comprising:

a first buffer in which is stored only first communication data sent from a first device connected to the first bus;

a first register in which is stored only first communication control information concerning the first communication data sent from the first device for handling the communication data, and when writing of the first communication data is completed, data end information is written as the first communication control information;

a second buffer in which is stored only second communication data sent from a second device connected to the second bus;

a second register in which is stored only second communication control information concerning the second communication data sent from the second device for handling the communication data, and when writing of the second communication data is completed, data end information is written as the second communication control information; ~~and~~

a status register storing information indicating a status of the first buffer, the first register, the second buffer, and the second register, the status indicating that the first buffer is full of data, the second buffer is full of data, new information has been written in the first register, and new information has been written in the second register; and

a control circuit passing the first communication data stored in said first buffer to the second device and the first ~~communication control~~ data end information stored in said first register to the second device, and further passing the second communication data stored in said second buffer to the first device and the second ~~communication control~~ data end information stored in said second register to the first device, wherein the first and second communication control information are sent via the first and second

registers, respectively, and the first and second communication data are sent via the first and second buffers, respectively, ~~and~~ the first device reads out data stored in the second buffer if the status register indicates that the second register is full of data and that new information has been written in the second register, ~~and~~ the second device reads out data stored in the first buffer if the status register indicates that the first buffer is full of data, and that new information has been written in the first register, and the first device and the second device, and the first device and the second device perform an appropriate receive process according to the second and first control information, respectively, and complete the receive process when detecting the data end information.

7. (Currently Amended) An information processing unit for carrying out information processing in cooperation with an external host apparatus connected thereto via an external connection bus, comprising:

an internal CPU;

a receive buffer in which is stored only receive data received from said external host apparatus;

a receive register in which is stored only receive communication control information concerning the receive data from said external host apparatus for handling the receive data, and when the receive data ends, data end information is written as the receive communication control information;

a transmit buffer in which is stored only transmit data transmitted from said internal CPU via an internal bus;

a transmit register in which is stored only transmit communication control information concerning the transmit data from said internal CPU for handling the transmit data, and when writing of the transmit data is completed, data end information is written as the transmit communication control information; ~~and~~

a status register storing information indicating a status of the receive buffer, the receive register, the transmit buffer, and the transmit register, the status indicating that the receive buffer is full of data, the transmit buffer is full of data, new information has been written in the receive register, and new information has been written in the treatment register; and

a control circuit for passing the receive data stored in said receive buffer to said internal CPU and passing the receive communication control information stored in said receive register to said internal CPU, and further passing the transmit data stored in said transmit buffer to said external host apparatus and passing the transmit communication control information stored in said transmit register to said external host apparatus, wherein the receive data and receive communication control information are sent via the receive buffer and receive register, respectively, and the transmit data and transmit communication control information are sent via the transmit buffer and transmit register, respectively, and wherein said internal CPU reads out data stored in the receive buffer if the status register indicates that the receive buffer is full of data and if the status register indicated that new information has been written in the receive register, ~~and~~ said external host apparatus reads out data stored in the transmit buffer if the status register indicates that the transmit buffer is full of data, and that new information has been in the transmit register, and said internal CPU and said external

host apparatus perform an appropriate process according to the control information and complete the process when detecting the data end information.

8. (Original) The information processing unit as claimed in claim 7, wherein said control circuit outputs an interrupt signal to said internal CPU, when said receive buffer is full of the receive data, or when the receive communication control information is stored in said receive register.

9. (Original) The information processing unit as claimed in claim 8, further including a status register for storing information indicative of whether or not untransmitted data exists in said receive register,

wherein said control circuit updates the information in said status register, when new data is stored in said register, or when data in said buffer is read out by the second device, and

wherein said internal CPU refers to the information in said status register when said internal CPU receives the interrupt signal.

10. (Original) The information processing unit as claimed in claim 7, wherein said control circuit outputs a transmit data-related request signal for requesting reception of the transmit data, to said external host apparatus, when data is stored in said transmit buffer or said transmit register.

11. (Withdrawn) An external host apparatus for carrying out processing in cooperation with an information processing unit for performing specific information processing, comprising:

data-reading means for reading transmit data into a transmit buffer within the information processing unit by designating an address of the transmit buffer in response to a transmit data-related request signal for requesting reception of transmit data outputted from the information processing unit, and reading transmit communication control information into a transmit register within the information processing unit by designating an address of the transmit register; and

data-writing means for writing receive data into a receive buffer within the information processing unit by designating an address of the receive buffer in response to a receive data-related request signal outputted from the information processing unit for indicating that data can be received, and writing receive communication control information into a receive register within the information processing unit by designating an address of the receive register.

12. (Withdrawn) The external host apparatus as claimed in claim 11, wherein said data-writing means writes data end information for notifying the external host apparatus that writing of the receive data has been terminated, as the receive communication control information, when the writing of the receive data has been completed.

13. (Withdrawn) A method of controlling inter-bus communication control for carrying out data communication between a first device connected to a first bus and a second device connected to a second bus, via an inter-bus communication interface device,

the method comprising the steps of:

causing the first device to store communication data to be passed to the second device in a buffer within the inter-bus communication interface device;

causing the first device to store communication control information concerning the communication data in a register within the inter-bus communication interface device;

causing the inter-bus communication interface device to output an interrupt signal to the second device, when the buffer is full of the communication data, or when the communication control information is stored in said register; and

causing the second device to read out the communication data in the buffer or the communication control information in the register in response to the interrupt signal.

14. (Withdrawn) The method as claimed in claim 13, wherein the first device writes data end information notifying the second device that writing of the communication data has been terminated, as the communication control information, and

wherein the second device reads the data end information, thereby recognizing termination of the writing of the communication data.

15. (Withdrawn) A data security device for carrying out processing for securing data, comprising:

a data-acquiring circuit for acquiring data to be processed;

a cryptographic processing circuit for performing cryptographic processing of input data; and

a data input/output control circuit connected to said data-acquiring circuit via a first bus and connected to said cryptographic processing circuit via a second bus, for acquiring the data to be processed which is acquired by said data-acquiring circuit via the first bus, for storage in an internal memory thereof, inputting the data to be processed to said cryptographic processing circuit via the second bus, and acquiring result data as a result of execution of the cryptographic processing from said cryptographic processing circuit via the second bus.

16. (Withdrawn) The data security device as claimed in claim 15, wherein said data input/output control circuit includes a direct memory access controller provided for the first bus, and acquires the data to be processed from said data-acquiring circuit by Direct Memory Access transfer.

17. (Withdrawn) The data security device as claimed in claim 15, further comprising a memory device connected to the first bus, for storing the data to be processed which is acquired by said data-acquiring circuit, and

wherein said data input/output control circuit obtains the data to be processed from said memory device.

18. (Withdrawn) The data security device as claimed in claim 15, wherein after storing the data to be processed in said memory device, the data to be processed is divided into unit data each having a unit data length and serving as a unit for the cryptographic processing, and then inputted to said cryptographic processing circuit.

19. (Withdrawn) The data security device as claimed in claim 18, wherein said memory device is divided into at least two areas, and while the data to be processed which is stored in a first area is being processed by said cryptographic processing circuit, following data of the data to be processed is stored in a second area.

20. (Withdrawn) The data security device as claimed in claim 19, wherein said internal memory is divided into areas each having a unit storage capacity corresponding to the unit data length of the unit data for the cryptographic processing.

21. (Withdrawn) The data security device as claimed in claim 15, wherein said data input/output control circuit inputs the data to be processed which is sequentially provided though streaming, to said cryptographic processing circuit in an order of acquiring of the data to be processed, and outputs result data as a result of execution of the cryptographic processing whenever the result data is acquired.

22. (Withdrawn) The data security device as claimed in claim 15, wherein said cryptographic processing circuit detects a volume of input data to be processed, and

carries out the cryptographic processing on the data to be processed when the volume of the input data to be processed reaches predetermined value.

23. (Withdrawn) The data security device as claimed in claim 15, wherein a plurality of said cryptographic processing circuits are provided such that a plurality of said data input/output control circuits are connected to said plurality of said cryptographic processing circuits in a manner individually associated therewith, respectively, and wherein said plurality of said data input/output control circuits acquire the data to be processed as divisional formed by dividing the data to be processed, and input the divisional data to said corresponding cryptographic processing circuits in parallel with each other.

24. (Withdrawn) The data security device as claimed in claim 15, further comprising an authentication processing circuit for carrying out authentication processing of input data, and

wherein said data input/output control circuit is connected to said authentication processing circuit via a third bus, and wherein said data input/output control circuit inputs the data to be processed which is to be subjected to the cryptographic processing, to said cryptographic processing circuit, and inputs the data to be processed which is to be subjected to the authentication processing to said authentication processing circuit.

25. (Withdrawn) A data security device for carrying out processing for securing data, comprising:

a data-acquiring circuit for acquiring data to be processed;

an authentication processing circuit for performing authentication processing of input data; and

a data input/output control circuit connected to said data-acquiring circuit via a first bus and connected to said authentication processing circuit via a second bus, for acquiring the data to be processed which is acquired by said data-acquiring circuit via the first bus, for storage in an internal memory thereof, and inputting the data to be processed to said authentication processing circuit via the second bus.

26. (Withdrawn) A data communication device for transmitting/receiving secured data via a network, comprising:

a main CPU for generating transmit data;

a cryptographic processing circuit for encrypting input data;

a communication circuit for transmitting the input data via the network; and

a data input/output control circuit connected to said main CPU and said communication circuit via a first bus and connected to said cryptographic processing circuit via a second bus, for acquiring the transmit data acquired by said main CPU via the first bus, for storage in an internal memory thereof, inputting the transmit data to said cryptographic processing circuit via the second bus, acquiring encrypted data from said cryptographic processing circuit via the second bus, and inputting the encrypted data to said communication circuit.

27. (Withdrawn) A data communication device for transmitting/receiving secured data via a network, comprising:

a main CPU for processing receive data;

a cryptographic processing circuit for decrypting input data;

a communication circuit for acquiring the receive data transmitted via the network; and

a data input/output control circuit connected to said main CPU and said communication circuit via a first bus and connected to said cryptographic processing circuit via a second bus, for acquiring the receive data acquired by said communication circuit via the first bus, for storage in an internal memory thereof, inputting the receive data to said cryptographic processing circuit via the second bus, acquiring plaintext data after decryption from said cryptographic processing circuit via the second bus, and inputting the plaintext data to said main CPU.

28. (Withdrawn) A method of securing data security method for securing data, comprising the steps of:

causing a data input/output control circuit to acquire data to be process which is acquired by a data-acquiring circuit, via a first bus, for storage in an internal memory thereof;

causing the data input/output control circuit to input the data to be processed to a cryptographic processing circuit via a second bus;

causing the cryptographic processing circuit to carry out cryptographic processing of the data to be processed; and

passing result data as a result of execution of the cryptographic processing from the cryptographic processing circuit to the data input/output control circuit.

29. (Withdrawn) A method of securing data, comprising the steps of:

causing a data input/output control circuit to acquire data to be process which is acquired by a data-acquiring circuit, via a first bus, for storage in an internal memory thereof;

causing the data input/output control circuit to input the data to be processed to an authentication processing circuit via a second bus; and

causing the authentication processing circuit to carry out authentication processing of the data to be processed.